3D Optimization of Ferrite Inductor Considering Hysteresis Loss

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1. **Introduction**
   - A) Background
   - B) Purpose
2. Coupled analysis
3. 3D shape optimization of Inductor
4. Conclusion

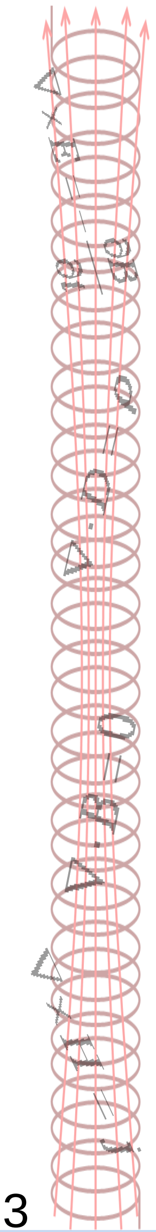
Background

- Dc-dc converters

⇒ They are used for electric and electronic devices,
Their efficiency must be improved.

- The energy losses in dc-dc converters are caused in
  - control ICs
  - FETs and diodes
  - Inductors

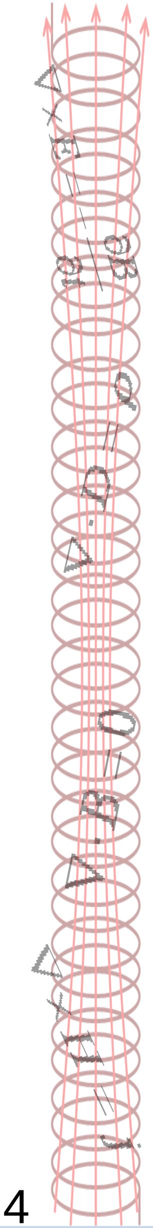
⇒ The purpose of this work is that the efficiency of the dc-dc converters is improved by ***reducing the inductor losses***.



Purpose

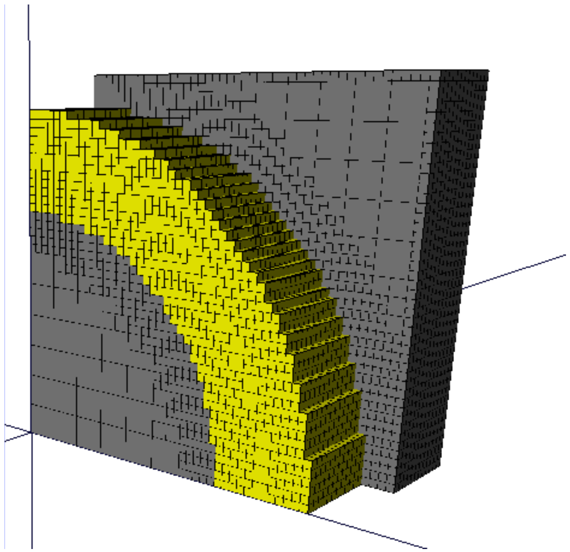
- The losses in the inductors are
  - <u>Copper loss due to the winding resistance,</u>
  - <u>Hysteresis loss due to the magnetic cores.</u>
- The inductors must be designed to reduce them simultaneously under the condition that the inductance satisfies the specifications for inductance.
- Design optimization based on the finite element analysis is effective to solve this problems

- However, optimizations of 3D inductor models are computationally ***prohibitive*** mainly due to time consuming mesh generations.
- We **present the 3D shape optimization of the inductor** on the basis of nonconforming voxel FEM.



(Introduction. B): Purpose

- In the present method, the voxels at the material boundaries are subdivided into fine voxels.
  - The fine voxels at the boundaries improve the accuracy in the voxel FEM.
  - This method realizes ***fast generation of FE meshes***.



⇨ The *multiobjective optimization of the inductors* is performed to minimize the copper and hysteresis.

1. **Introduction**
2. **Coupled analysis**
    - A) Dc-dc converter model
    - B) Inductance under dc bias
    - C) Hysteresis loss
    - D) Inductor model for test
    - E) Analysis results
3. 3D shape optimization of Inductor
4. Conclusion

Dc-dc converter model

- Before the optimizations, we evaluate the **inductance and hysteresis loss under the dc bias condition** by performing the ***coupled analysis*** of inductors and dc-dc converters.
  - A boost circuit shown in Fig 1 is analyzed.
    - The steady-state mode is evaluated.
    - The FET and diode are treated as ideal devices, except for their on-resistance.
    - The hysteresis loss is evaluated using the Steinmetz formula in the post processing.

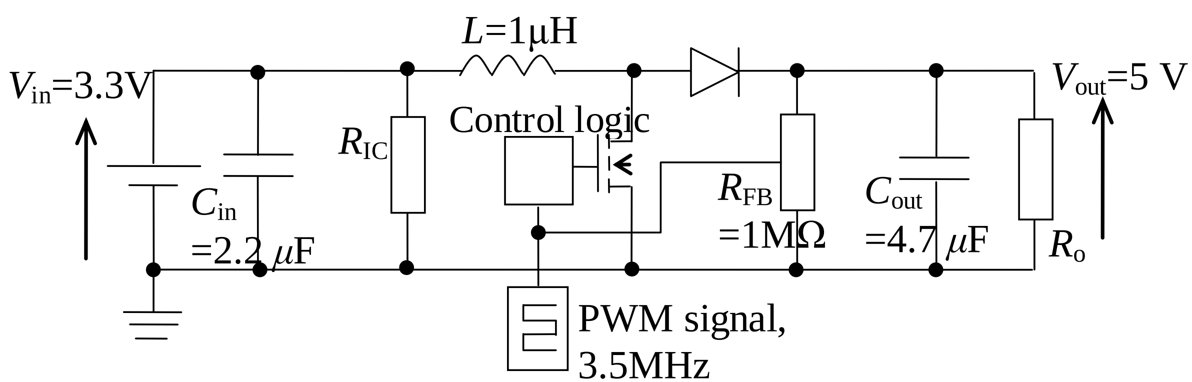


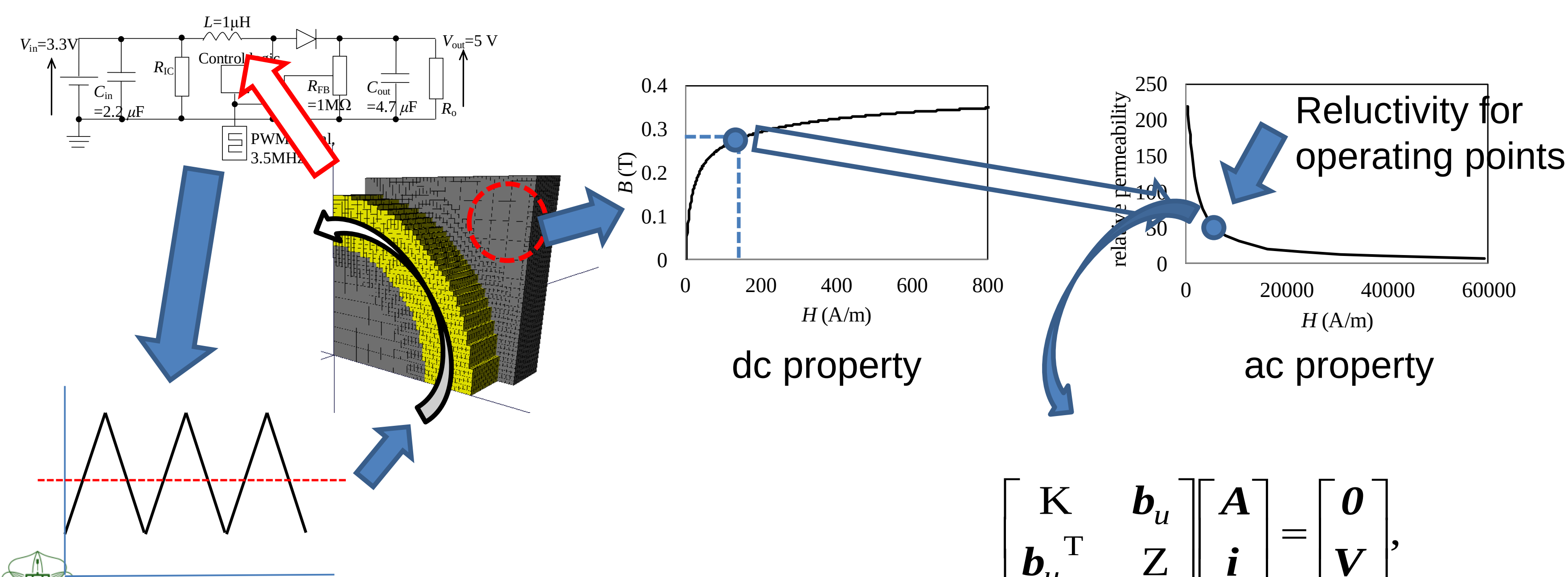
Fig. 1 Boost circuit.

Inductance under dc bias

1. (***Circuit analysis***): Assuming the value of inductance and winding resistance in the inductor, the circuit analysis of the boost circuit is carried out.

2. (***Nonlinear FEM***): The operating points in FEs corresponding to the dc bias are computed based on the nonlinear analysis using the dc property.

3. (***Coupled analysis***): The reluctivity for the operating points is determined from the ac property. The coupled analysis is performed over one cycle around the operating point, in which magnetic field is analyzed by the linear FE equation using the determined reluctivity.



$$\begin{bmatrix} K & \boldsymbol{b}_u \\ \boldsymbol{b}_u^{T} & Z \end{bmatrix} \begin{bmatrix} \boldsymbol{A} \\ \boldsymbol{i} \end{bmatrix} = \begin{bmatrix} \boldsymbol{0} \\ \boldsymbol{V} \end{bmatrix},$$

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Hysteresis loss

- The hysteresis loss in the inductor, W_h (W), is estimated based on the Steinmetz formula using the coupled analysis results.

$$W_h = K_h f \sum_e V_e \|\boldsymbol{B}_e\|^{\alpha}$$

K_h [W/(m^3·s)]$=9945.7$, $\alpha=2.26$: hysteresis coefficients

f : switching frequency, V_e : volume of element e

$\boldsymbol{B}_e$: amplitude of flux density in element e

- K_h and α are measured under the condition that f is 3.5MHz.

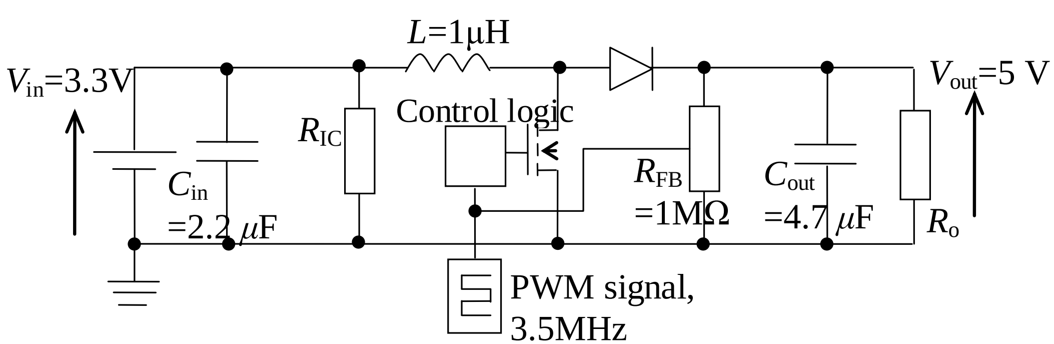
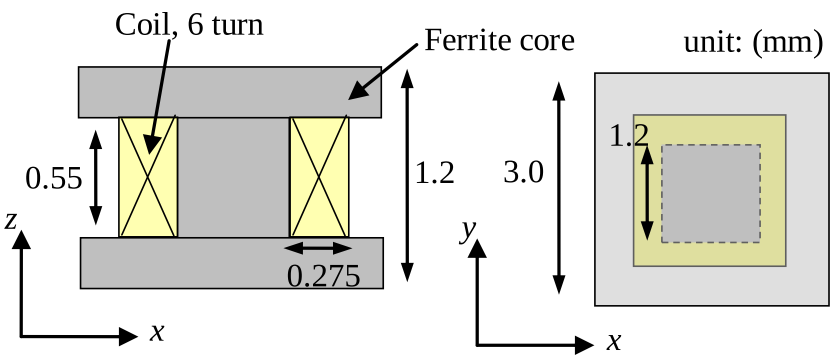


Fig. 1 Boost circuit.

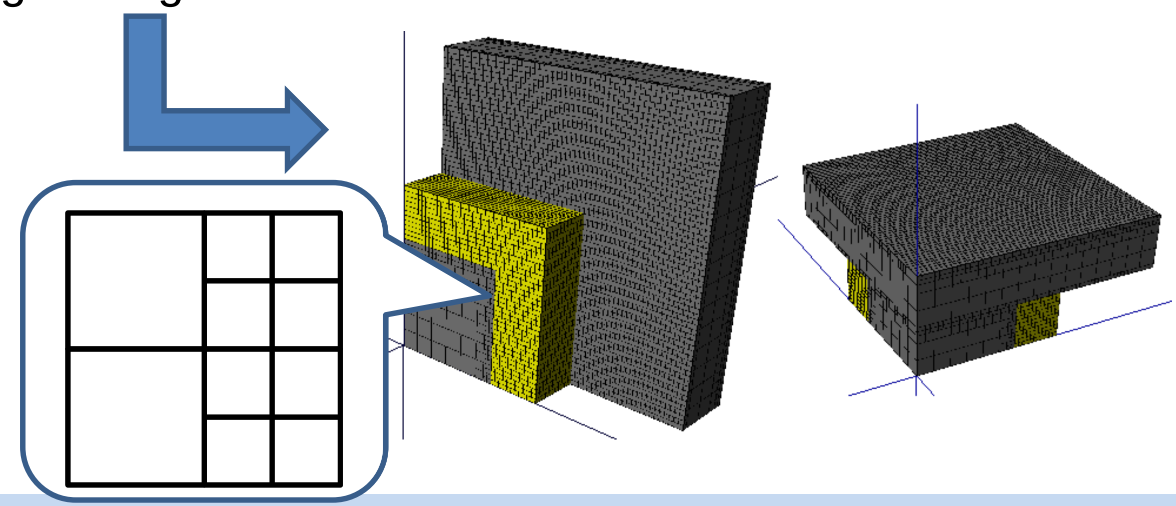
Inductor model

- To test the validity of the analysis, the efficiency of the boost circuit in the steady-state mode is computed.
- The inductor shown in Fig. 2 is used in the circuit.



- Inductance：1.09(μH)
- Winding resistance:0.14(Ω)

Fig. 2 Original model

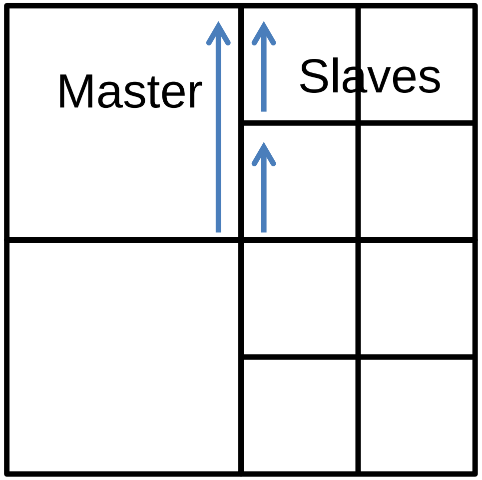


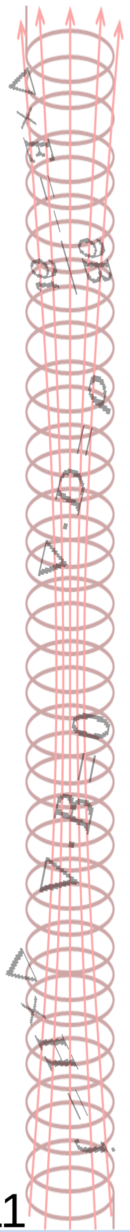
Nonconforming connections

- In the FE analysis, the unknowns assigned to nonconforming edges (slave edge) are interpolated by those assigned to the conforming edges (master edge).
- Slave unknown, A_s, is expressed by the linear combination of the master unknowns.

$$A_s = \sum_{i=1} A_i^m \int_{e_s} \boldsymbol{N}_i^m \cdot dl$$

A_i^{m}: master unknowns $\boldsymbol{N}_i^{\mathrm{m}}$: interpolated function l: tangential vector of slave





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- The simulation results and measurement data are shown in Fig. 3.
  - ✓ The simulation results are in good agreement with the measurement results. The efficiency in the heavy load conditions obtained by the analysis and measurement is almost identical.
  - ✓ There exist small discrepancies for the light load conditions. This would be due to the fact that turn-on and off times in FET are not taken into account.

⇒ The inductance and hysteresis loss, as well as the copper loss, under the bias condition are correctly considered

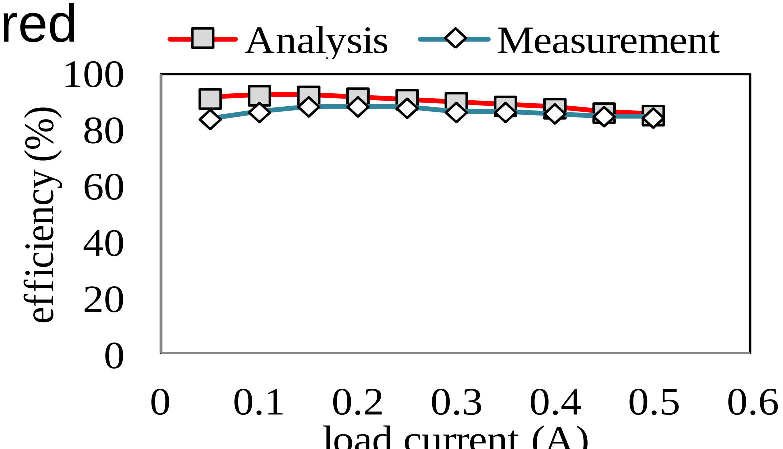


Fig. 3 Efficiency.

Analysis results

- Fig. 4 shows the computed hysteresis and copper losses.
- Hysteresis loss is dominant in the light loads, whereas the copper loss is dominant in the heavy loads.
- The inductor current is shown in Fig. 5.
- The amplitudes of the current are about 320mA being independent of the load resistance.

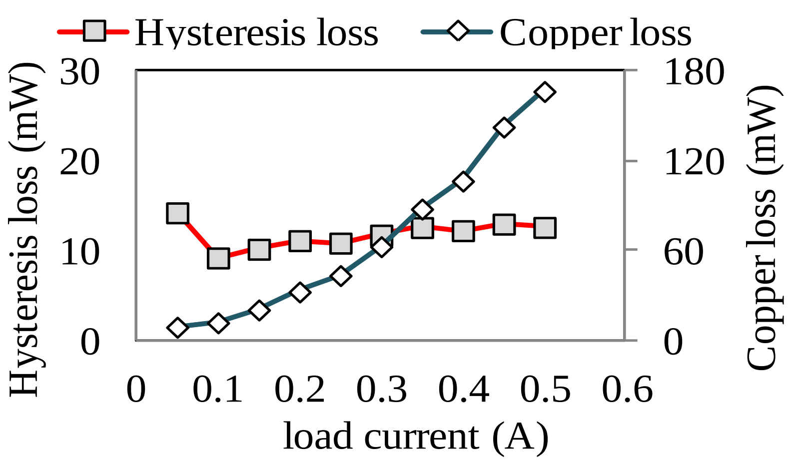


Fig. 4 Hysteresis. and Copper losses

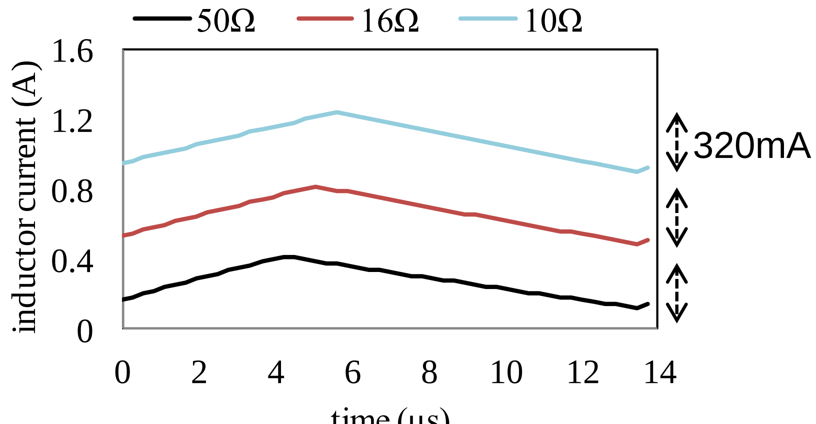
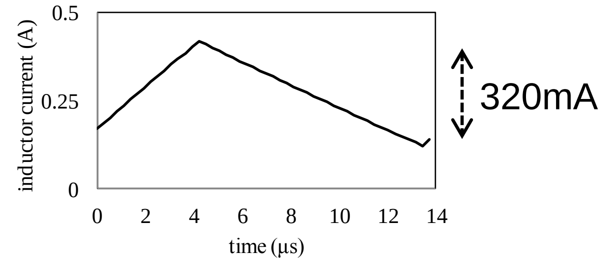


Fig. 5 Inductor current

Analysis for optimization

- If the hysteresis loss is evaluated using the coupled analysis, long computational time is necessary in the optimizations.

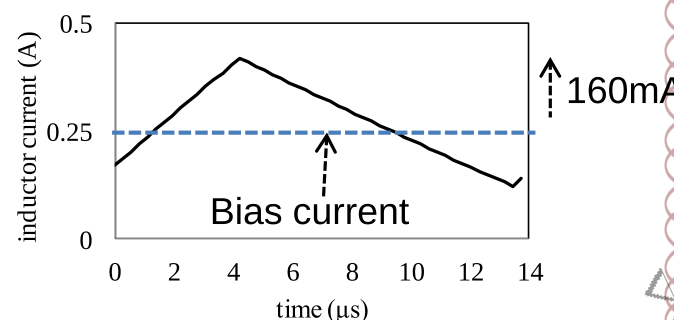
> ✓ The inductor current is independent of the load resistance.
>
> ✓ We use Steinmetz formula.



$$W_h = K_h f \sum_e V_e \left\| \boldsymbol{B}_e \right\|^{\alpha}$$

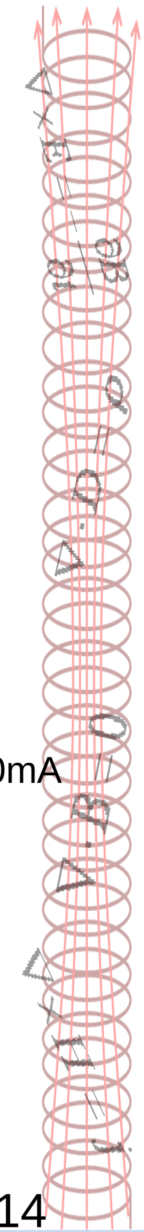
- The hysteresis loss is estimated only by the magnetostatic analysis.

1. The operating points in FEs for a bias current are computed.
2. Linearized FE equation around the operating point is solved, in which the inductor current is set to 160mA.



From the resultant flux density, the hysteresis loss can be evaluated, in addition to the inductance.

$$W_h = K_h f \sum_e V_e \left\| \boldsymbol{B}_e \right\|^{\alpha}$$



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    - A) Optimized inductor model
    - B) Objectives
    - C) Optimization results
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Optimized inductor model

- The inductor shown in Fig. 6 is optimized.
  - Design variables $\boldsymbol{g}$: five parameters

$$\boldsymbol{g} = [r_1 \quad r_2 \quad c_h \quad w \quad c_r]^{\mathrm{T}}$$

c_r is the diameter of the winding wire, which takes 0.1 or 0.15mm.

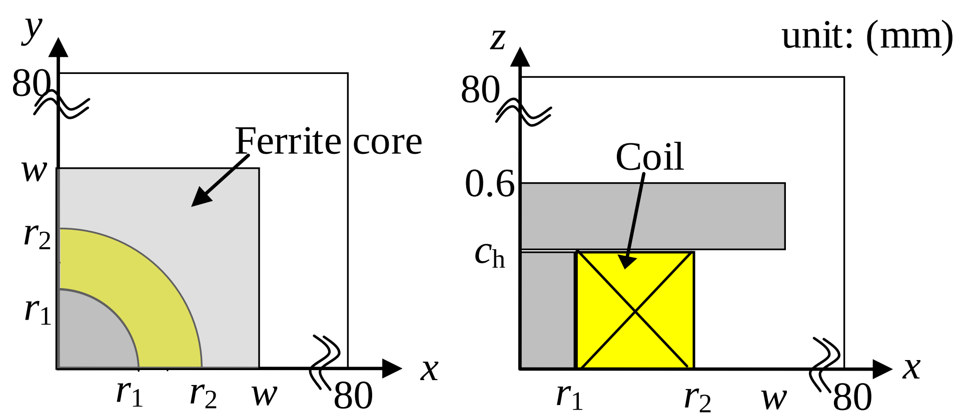


Fig. 6 Optimized inductor model (1/8)

Objectives

- Two objective functions and constraints are defined.

Objectives: $f_1 = R, \quad f_2 = W_h,$

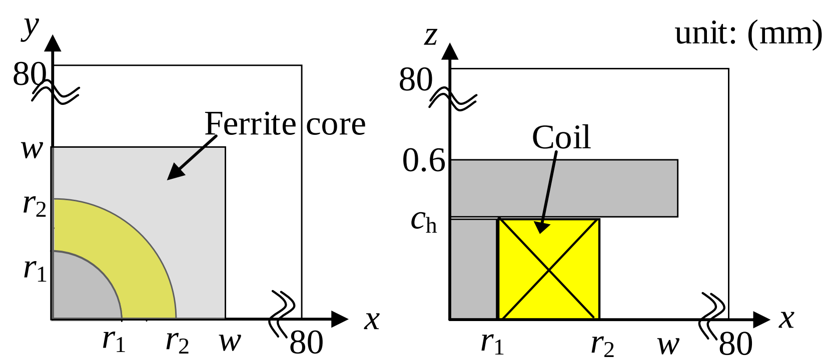
constraints: $\dfrac{(L - L_T)^2}{L_T{}^2} < 0.03, \quad L_l > 0.7L_T, \quad r_2 < w < 1.5\text{mm}$

R (Ω): winding resistance, W_h (mW): Hysteresis loss.

L_T=1μH: specified inductance.

L (μH): inductance value when dc bias is 0.2A.

L_l (μH) : inductance value when dc bias is 2.7A.



optimization results

- The optimization is performed using the real-ceded Generic Algorithm and Strength Pareto Evolutionally Algorithm 2.
- The optimization is performed over 200 generations.
  - The Pareto solutions are shown in Fig. 6 in which the red and blue makers denote the solutions with c_r=0.15 and 0.1 mm, respectively.
  - All Pareto solutions are superior to the original inductor.

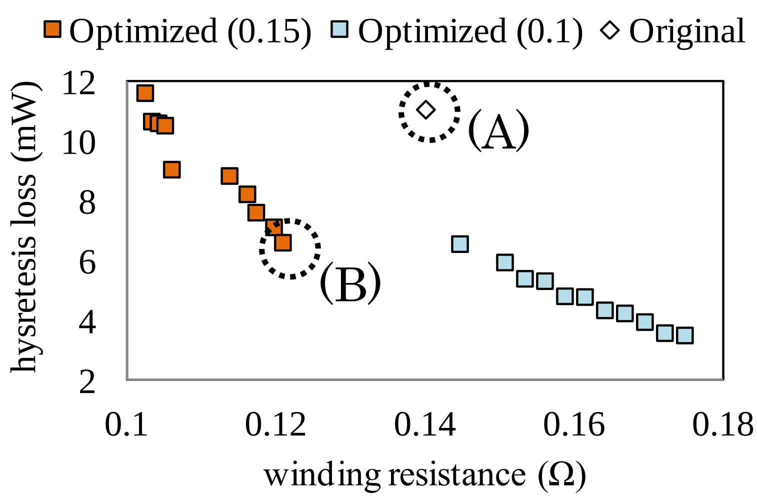
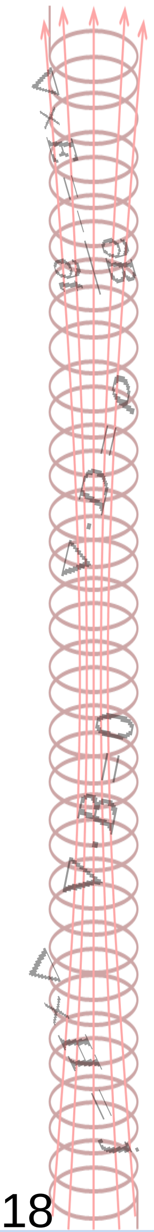


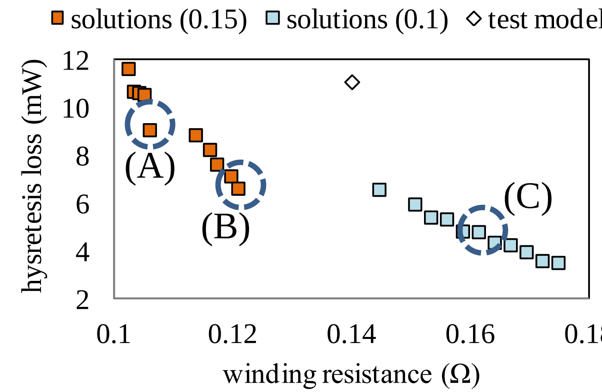
Fig. 8 Pareto solutions

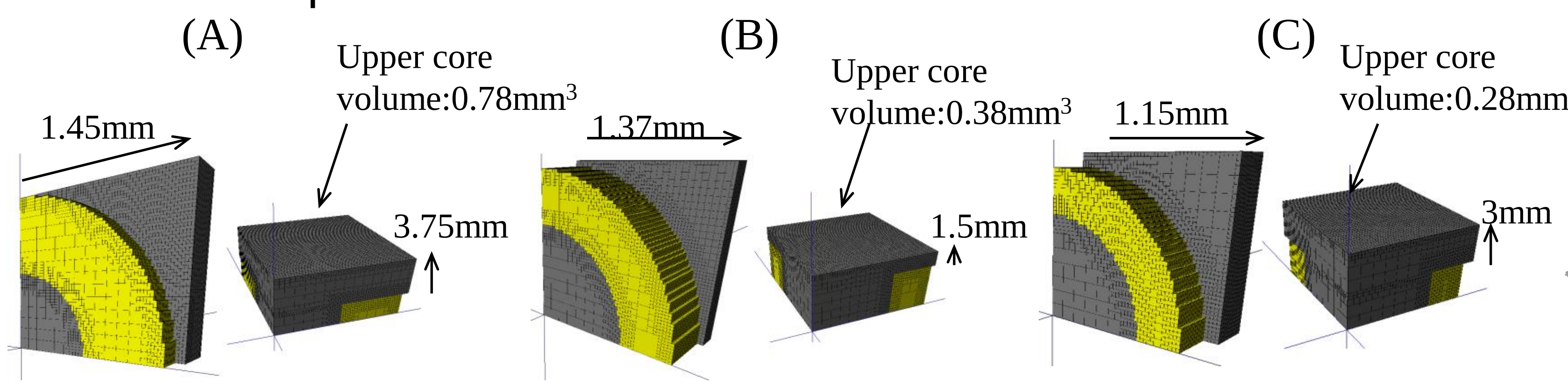


optimization results

- The resultant inductor shapes are shown below.

  - Shape(A) has large cross-section of the coil. The cross-section on the cylindrical core is so small that the magnetic induction is strong here and hysteresis loss is large.
  - Shape (C) has small and large cross-sections of the coil and cylindrical core, respectively.
  - Shape (B) is in between (A) and (C). This seems to be optimum in this case.





(A) L: 0.976μH, L_l: 0.96μH, R: 10.5mΩ, W_h: 9.08mW, Num. turn: 3

(B) L: 0.97μH, L_l: 0.94μH, R: 12.07mΩ, W_h: 6.67mW, Num. turn: 4

(C) L: 0.99μH, L_l: 0.98μH, R: 16.1mΩ, W_h: 4.8mW, Num. turn: 4

optimization results

- The circuit efficiency is computed for the shape (B).
  - Because both losses in the inductor are reduced, the **efficiency in the all loads is improved.**
  - It can be concluded that the present method can find the inductor to improve the efficiency of the converter.

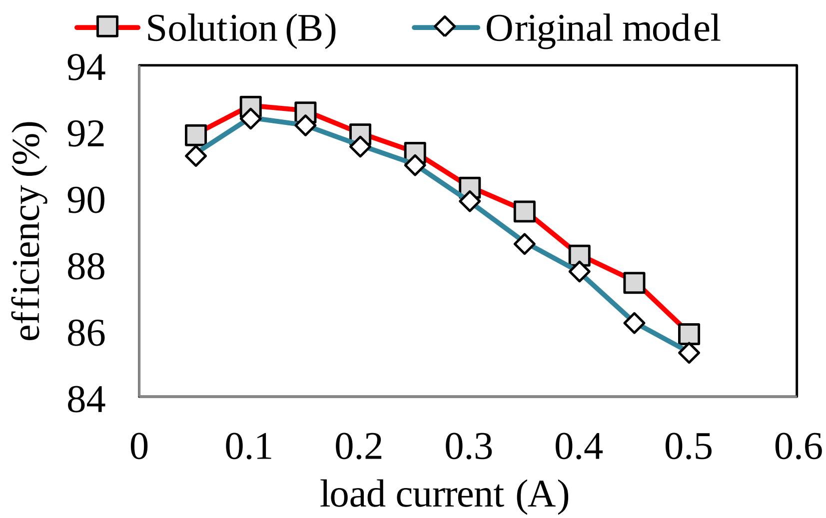


Fig. 9 Efficiency after optimization.

1. Introduction

2. Coupled analysis

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4. **Conclusion**

Conclusions

- The efficiency in the dc-dc converters must be improved.
  - The hysteresis and copper losses in the inductors should be minimized.
- Multiobjective optimization of 3D inductor shape is performed based on the nonconforming voxel FEM.
- The hysteresis loss and winding resistance can be reduced under the restriction that the inductance satisfies the specifications.
- The circuit efficiency is improved using the resultant inductor.

Future works

- Hysteresis modeling is introduced for the accurate analysis.